IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently Amended): A semiconductor device comprising:

a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type formed on the first semiconductor region;

a third semiconductor region of the first conductivity type formed on a part of the second semiconductor region;

a trench formed to range from a surface of the third semiconductor region to the third semiconductor region and the second semiconductor region, the trench penetrating the third semiconductor region, a depth of the trench being shorter than a depth of a deepest bottom portion of the second semiconductor region, and the trench having no second semiconductor region under its bottom surface;

a gate insulating film formed on both facing side surfaces of the trench;

first and second gate electrodes formed on the gate insulating film ~~on~~ and opposed to the ~~respective~~ facing side surfaces of the trench, the first and second electrodes being separated from each other; and

a first conductive material formed between the first and second gate electrodes on the side surfaces of the trench, with an insulating film intervened between the first conductive material and the first and second gate electrodes.

Claim 2 (Original): A semiconductor device according to claim 1, further comprising a fourth semiconductor region of the first conductivity type formed between the bottom surface of the trench and the first semiconductor region, the fourth semiconductor region

having an impurity concentration higher than an impurity concentration of the first semiconductor region.

Claim 3 (Original): A semiconductor device according to claim 2, the fourth semiconductor region being arranged apart in boundary regions of the first semiconductor region and the second semiconductor region.

Claim 4 (Original): A semiconductor device according to claim 1, further comprising: a fifth semiconductor region of the second conductivity type formed on a part of the second semiconductor region, the fifth semiconductor region having an impurity concentration higher than an impurity concentration of the second semiconductor region; and a source electrode formed on the fifth semiconductor region and the third semiconductor region.

Claim 5 (Original): A semiconductor device according to claim 4, the first conductive material being electrically connected to the source electrode.

Claim 6 (Original): A semiconductor device according to claim 1, the first conductive material being a floating electrode.

Claim 7 (Currently Amended): A semiconductor device according to claim 1, the separated first and second gate electrodes being connected to each other at a part thereof inside the trench above a non-inversion region beneath the trench.

Claim 8 (Original): A semiconductor device according to claim 7, further comprising a sixth semiconductor region of the second conductivity type formed between the first

semiconductor region and a bottom surface of the trench located under the part, at which the separated first and second gate electrode are connected, the sixth semiconductor region having an impurity concentration higher than an impurity concentration of the second semiconductor region.

Claim 9 (Withdrawn): A semiconductor device according to claim 1, further comprising an insulating film formed between the bottom surface of the trench and the separated first and second gate electrodes, and between the bottom surface of the trench and the first conductive material, and insulating film having a film thickness greater than a thickness of the gate insulating film formed on the side surfaces of the trench.

Claim 10 (Original): A semiconductor device according to claim 1, the first semiconductor region forming a drain region, the second semiconductor region forming a base region, and the third semiconductor region forming a source region, and the first to third semiconductor regions being formed into a MOS field-effect transistor.

Claim 11 (Withdrawn): A semiconductor device according to claim 1, further comprising a second conductive material formed under the first conductive material and extending below the first and the second gate electrodes.

Claim 12 (Withdrawn): A semiconductor device comprising: a first semiconductor region of a first conductivity type;

a second semiconductor region of a second conductivity type formed on the first semiconductor region;

a third semiconductor region of the first conductivity type formed on the second semiconductor region;

a trench penetrating the third semiconductor region and the second semiconductor region from a surface of the third semiconductor region, a depth of the trench being shorter than a depth of a deepest bottom portion of the second semiconductor region;

a gate insulating film formed on both facing side surfaces of the trench;

a gate electrode formed on the gate insulating film in the trench; and

an insulating film formed between a bottom surface of the trench and the gate electrode, the insulating film having a film thickness greater than a thickness of the gate insulating film formed on the side surfaces of the trench.

Claim 13 (Withdrawn): A semiconductor device according to claim 12, further comprising a fourth semiconductor region of the first conductivity type formed between the bottom surface of the trench and the first semiconductor region, the fourth semiconductor region having
an impurity concentration higher than an impurity concentration of the first semiconductor region.

Claim 14 (Withdrawn): A semiconductor device according to claim 13, the fourth semiconductor region, formed between the bottom surface of the trench and the first semiconductor region, being arranged apart in boundary regions of the first semiconductor region and the second semiconductor region.

Claim 15 (Withdrawn): A semiconductor device according to claim 12, further comprising: a fifth semiconductor region of the second conductivity type formed on a part of

the second semiconductor region, the fifth semiconductor region having an impurity concentration higher than an impurity concentration of the second semiconductor region; and a source electrode formed on the fifth semiconductor region and the third semiconductor region.

Claim 16 (Withdrawn): A semiconductor device according to claim 15, the conductive material being electrically connected to the source electrode.

Claim 17 (Withdrawn): A semiconductor device according to claim 12, the first semiconductor region forming a drain region, the second semiconductor region forming a base region, and the third semiconductor region forming a source region, and the first to third semiconductor regions being formed into a MOS field-effect transistor.

Claim 18 (Withdrawn): A method of manufacturing a semiconductor device, comprising:

forming a first semiconductor region on a semiconductor substrate;

forming a trench of a predetermined depth in the first semiconductor region;

forming a second semiconductor region on a surface region of the first semiconductor region, the second semiconductor region contacting side surfaces of the trench;

forming a gate insulating film on the facing side surfaces of the trench;

depositing a conductive film on the gate insulating film;

subjecting the conductive film to anisotropic etching, and leaving the conductive film only on the side surfaces of the trench; and

ion-implanting impurities into the first semiconductor region by self alignment, with the conductive film on the side surfaces of the trench used as a mask, and forming a fourth semiconductor region under a bottom surface of the trench.